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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,536	01/15/2004	Supat Wongwirawat	14587	4565

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Ralph A. Dowell of DOWELL & DOWELL P.C.
2111 Eisenhower Ave
Suite 406
Alexandria, VA 22314

EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,536	WONGWIRAWAT ET AL.	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after t he mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 10, 12, 14 - 16, 19 - 44, 46* is/are rejected.

7)☒ Claim(s) *11, 13, 17 - 18, 45, 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 35 is objected to because of the following informalities: A repeat of "of said" has been observed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 25 – 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 25 recites the limitation "*remaining*" phase error. It is not clear from the claim that there was a previous phase error in order to determine a remaining phase error.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 5, 14 – 15, 23 – 26, 33, 36 and 38 - 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Ke et al. (US 6,696,886).

Re claim 1, Ke teaches of a digital receiver for demodulating a digital signal modulated onto a carrier (Fig.2), comprising: a tuner (#210, Col 5, Lines 16 – 24); an analog to digital converter, for digitizing a channel tuned by said tuner to provide a digitized channel (#220, Fig.2, Col 5, Lines 25 – 29); a coarse carrier recovery circuit for extracting said digital signal from said digitized channel at near baseband (#230 and #240, Fig.2, Col 5, Lines 27 – 32); a feed forward equalizer receiving said digital signal at near baseband and outputting a feed forward equalized signal (#250, Fig.2, Col 5, Lines 32 – 35); a fine carrier recovery circuit (#200, Fig.2) for phase shifting (#115, Fig.2) said feed forward equalized signal by a phase correction angle to adjust for

remaining offsets in phase and frequency of said feed forward equalized signal attributable to phase and frequency offsets in said carrier (Col 5, Lines 35 – 56 and Col 6, Lines 2 - 5); said fine carrier recovery circuit comprising a filter (#105, Fig.1) for filtering an estimate of a phase error (#130, Fig.1, Col 6, Lines 29 – 32) in said carrier to control said phase correction angle (#190, Fig.1, Col 6, Lines 49 – 54), wherein at least one filter parameter of said filter varies adaptively with said phase error (confidence value, Col 6, Lines 55 – 63). It should be noted that the frequency error Fe is included in the frequency tracking related portion of the phase error (Col 6, Lines 39 – 40).

Re claims 2 and 14 Ke teaches of a multiplier (phase derotator, #115, Fig.1) and a signal generator (#180, Fig.1) for generating a signal to multiply said feed forward equalized signal to phase shift (derotation) said feed forward equalized signal (Col 5, Lines 52 – 56).

Re claim 3, Ke teaches of a threshold slicer (#120, Fig.1) for determining a quantized modulated signal corresponding to said digital signal (Col 5, Lines 56 – 59).

Re claim 4, Ke teaches of multiplier comprises a sine generator (#180, Fig.1) for generating a signal representative of the sine ($\sin\theta_e$, Fig.1) of said phase correction angle (Col 7, Lines 1 – 10).

Re claim 5 and 39, Ke teaches of the filter comprising a phase-locked loop (Col 10, Lines 55 – 58) having an adjustable bandwidth (#105, Fig.6), varied adaptively with said estimate of said phase error (see claim 1).

Re claim 15, Ke teaches of a phase error detector (#135, Fig.6, Col 10, Lines 53 – 61) for estimating errors in real and imaginary (QAM, Col 5, Lines 7 – 8) components of said digital signal.

Re claims 23 and 36, Ke teaches of the digital signal comprising a quadrature amplitude modulated (QAM) signal (Col 5, Lines 7 – 8).

Re claim 24, Ke teaches of the receiver being formed as an integrated circuit (Fig.1).

Re claim 25, Ke teaches of a digital receiver for receiving a signal modulated onto a carrier (QAM, Col 5, Lines 7 – 8), a method comprising: reducing multi-path interference in said signal (Abstract, Lines 11 – 14), by filtering said signal through a feed-forward equalizer to produce a feed forward-equalized signal (#250, Fig.2, Col 5, Lines 32 – 35); determining an estimate of a phase error in said carrier (#130, Fig.1, Col

6, Lines 29 – 32); filtering said estimate through a filter (#105, Fig.1) having at least one adjustable filter parameter to produce a phase correction signal (#190, Fig.1, Col 6, Lines 49 – 54); varying said adjustable filter parameter with said estimate of phase error (confidence value, Col 6, Lines 55 – 63); multiplying said feed forward equalized signal by said phase correction signal to de-rotate said feed forward equalized signal (#115, Fig.1, Col 5, Lines 52 – 56).

Re claim 26, Ke teaches of the adjustable filter parameter comprising a bandwidth of said filter (#160, Fig.1, Col 6 Lines 65 – 67 to Col 7, Lines 1 – 2).

Re claim 33, Ke teaches of the feed forward equalized signal being input of a slicer (#129, Fig.1, Col 5, Lines 56 – 58) and at said slicer forming a quantized signal from said input (Fig.1).

Re claim 38, Ke teaches of a digital receiver for demodulating a digital signal modulated onto a carrier, to produce a demodulated digital signal (Fig.1 and 2), said receiver comprising: a de-rotator (#115, Fig. 1 and 2, Col 5, Lines 52 - 56) for phase shifting an equalized version (#250, Fig.2) of said digital signal by a phase correction angle (Col 6, Lines 49 – 54) to adjust for remaining offsets in phase and frequency of equalized version of said digital signal attributable to phase and frequency offsets in said carrier (Col 5, Lines 36 – 51); a filter (#105, Fig.1) in communication with said de-rotator (Col 6, Lines 8 – 18, Fig.1), for filtering an estimate of a phase error (Col 6, Lines

29 – 32) in said demodulated digital signal to control said phase correction angle (Col 6, lines 49 – 54), wherein at least one filter parameter of said filter varies adaptively with said phase error (confidence value, Col 6, Lines 55 – 63). It should be noted that the frequency error Fe is included in the frequency tracking related portion of the phase error (Col 6, Lines 39 – 40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6 – 10,12, 27 – 31, 40 – 44 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ke in view of Li et al.(US 6,868,129).

Re claims 6 – 8, 27 – 29 and 40 - 42, Ke teaches all the limitations of claim 5 as well as the phase-locked loop calculating said phase correction angle, as the estimate of said phase error (*from phase detector*) multiplied (#145, Fig.6) by an adaptive gain (K_i, Fig.6) from the adaptive gain controller (#160, Fig.6) (Col 7, Lines 30 – 32). However, Ke on his QAM receiver (Col 5, Line 8) does not specifically teach of extracting the imaginary portion of said estimate of said phase error.

Li teaches of demodulation of a radio receiver where phase correction is applied (Abstract). Li teaches of phase-locked loop (Fig.3, Col 5, Lines 6 – 11) calculates said phase correction angle (phase error signal), as a function of the imaginary portion of said estimate of said phase error from a complex square circuit (#78, Fig.3) multiplied by an adaptive gain (β_c., Fig.3) (Col 5, Lines 29 – 49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have extracted the imaginary portion of the complex signal of

Li's, which is proportional to the phase error to estimate the phase error correction signal.

Re claim 9, 30 and 43, Ke teaches of the adaptive gain controller calculates said adaptive gain for a current symbol using the imaginary portion of said estimate of said phase error for said current symbol (see claims 6 – 8) multiplied (#147, Fig.1) by an adaptive gain for a previous symbol (delay, #148, Fig.1) (Col 7, Lines 35 – 40).

Re claim 10, 31 and 44, Ke teaches of the adaptive gain controller calculating said adaptive gain based on said estimate of said phase error in order to minimize an error in said symbols as demodulated from said carrier (Abstract, Lines 11 – 14).

Re claim 12 and 46, Ke and Li teach all the limitations of claim 8. However, Ke does not teach of a low pass filter for filtering the adaptive gain.

Li teaches of a lowpass filter of a low pass filtered phase error signal (#84, Fig.3, Col 5, Lines 38 – 41).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used another lowpass filter to low-pass the adaptive gain for an improved quality of the signal.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ke and Li as applied to claims 15 and 6 and in further view of Ahn (US 6,671,339).

Ke teaches all the limitations of claim 15 except of the phase error detector having at least two modes of operation, for uniquely estimating errors in said imaginary component in each of said at least two modes.

Li teaches all the limitations of claim 6 wherein estimating errors in said imaginary component but does not teach of the modes of operation.

Ahn teaches of a lock detecting apparatus for a multimedia digital broadcasting receiver applicable to a channel equalizer as well as a carrier recovery unit (Abstract). To enhance a bit error rate (BER) of the system after a pull-in of a corresponding noise, the carrier recovery unit uses gear shifting. The gear shifting method shifts a phase error detection algorithm from a blind mode to a decision-directed mode, thereby gradually decreasing the noise bandwidth of a loop filter. Such mode conversion method may be divided into a manual and automatic methods (Col 1, Lines 24 – 30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used two modes of operation shifting a phase error detection algorithm from a blind mode to a decision-directed mode, gradually decreases the noise bandwidth of a loop filter.

Claims 19 – 22, 34 - 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ke in view of Endres et al.(US 6, 418,164)

Ke teaches all the limitations of claim 3 except for the use of a decision feedback equalizer.

Endres teaches of an adaptive equalizer for use in blind equalization systems to compensate for transmission channel distortion and noise in a digital communication system (Abstract, Lines 1 – 3). The equalizer (#30, Fig.1) and carrier recovery (#32, Fig.1) comprise (Fig.3) of an adder (#66, Fig.3), a feedback equalizer (#74), a forward equalizer (#60) and a slicer (#68). The decision feedback equalizer provides a filtered delayed version of said quantized modulated signal to an input of said threshold slicer and is implemented using an FIR filter imbedded in a feedback loop, which makes the overall loop have an infinite impulse response (Fig.3, Col 6, Lines 7 – 25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a decision feedback equalizer in combination with a decision feedforward equalizer to allow low signal processing complexity and powerful equalization to the input of the threshold slicer.

Re claim 20, Ke teaches of the estimate of phase error (#130, Fig.1) determined as a function of signals to said input of said slicer (from derotator, Fig.1) and said quantized modulated signals output by said slicer (Fig.1).

Re claim 21, Ke teaches of the estimate of phase error further determined as a function of said output of said fine carrier recovery circuit (#100, output from 100 is derotated and input to 130 for a phase error estimate).

Re claim 22 and 37, Ke teaches all the limitations of claim 1 except for the digital signal comprising a vestigial sideband modulated (VSB) signal.

Endres teaches of the receiver intended for both QAM and VSB. Since VSB signals modulate information in a single dimension (the amplitude of the RF carrier) the equalizer parameters are therefore constrained to be real numbers (Col 7, Lines 22 – 26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have extracted the real portion of the complex signal in the QAM receiver so that could be intended for VSB.

Re claim 34, Ke teaches all of the limitations of claim 33. However, Ke does not specifically teach of estimating a phase difference between a signal at said input of said slicer and said quantized signal.

Endres teaches of a phase detector (#46, Fig.2), loop filter (#44) and sine/cosine generator (#42) in combination with multiplier (#48) constituting a closed loop for recovering the frequency and phase of the carrier signal. The phase difference of input

signals (#49, Fig.2) and output signals (#52) of slicer (#50) is detected in phase detector (#46). The detected phase difference, filtered in loop filter (#44) controls the frequency and phase of the sine/cosine generator (#42) in a direction so as to reduce the detected phase difference between the input signals to the phase detector (#46) (Col 5, Lines 51 – 60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have estimated the phase difference between the input and output of the slicer so to control the frequency and phase of the sine/cosine generator in a direction so as to reduce the detected phase difference between the input signals to the phase detector.

Re claim 35, Ke teaches of filtering the quantized signal (#105, Fig.1), and feeding the filtered quantized signal back (back to the phase derotator, #115, Fig.1) to the input of the slicer to reduce multi-path interference in the signal (Abstract, Lines 11 – 14).

Allowable Subject Matter

Claims 11, 13, 17 – 18, 45 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER